Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin structure formed on the insulating layer, the fin structure having a first and second side surface;

a first spacer formed adjacent the first side surface, the first spacer acting as a first floating gate for the memory device;

a second spacer formed adjacent the second side surface, the second spacer acting as a second floating gate for the memory device;

a gate dielectric layer formed on the first and second spacers and contacting the insulating layer, the gate dielectric layer acting as an inter-gate dielectric for the memory device;

a first gate ~~formed on~~ contacting the insulating layer and disposed on a first side of the fin; and

a second gate ~~formed on~~ contacting the insulating layer and disposed on a second side of the fin opposite the first side, wherein the first and second gates are electrically isolated from each other.

2. (original) The memory device of claim 1, further comprising:

a source region and a drain region formed on the insulating layer and disposed adjacent a respective first and second end of the fin structure.

3. (original) The memory device of claim 2, further comprising:

an oxide layer formed on the first and second side surfaces of the fin, the oxide layer acting as a tunnel oxide layer for the memory device.

4. (original) The memory device of claim 3, wherein the oxide layer has a width ranging from about 10 Å to about 100 Å.

5. (previously presented) The memory device of claim 1, wherein the first and second gates are associated with corresponding memory cells that are programmed independently of each other.

6. (original) The memory device of claim 1, wherein each of the first and second spacers comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

7. (original) The memory device of claim 1, further comprising:

a dielectric cap comprising at least one of a nitride and an oxide formed over a top surface of the fin structure.

8. (original) The memory device of claim 1, wherein the insulating layer comprises a buried oxide layer and the fin structure comprises at least one of silicon and germanium.

9. (original) The memory device of claim 8, wherein the fin structure has a width ranging from about 100 Å to about 1000 Å.

10-13. (canceled)

14. (currently amended) A non-volatile memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having first and second side surfaces and a top surface;

an oxide layer formed on the first and second side surfaces of the conductive fin;

a first spacer formed adjacent the first side surface of the fin, the first spacer acting as a first floating gate electrode;

a first gate formed on the insulating layer, the first gate acting as a first control gate for the non-volatile memory device;

a second spacer formed adjacent the second side surface of the fin, the second spacer acting as a second floating gate electrode; ~~and~~

a second gate formed on the insulating layer, the second gate acting as a second control gate for the non-volatile memory device, wherein the first and second gates are formed on opposite sides of the conductive fin and are electrically isolated from each other; and

an inter-gate dielectric formed between the first spacer and the first gate and between the second spacer and the second gate, wherein the inter-gate dielectric contacts the insulating layer.

15-16. (canceled)

17. (previously presented) The non-volatile memory device of claim 14, wherein the first and second spacers each comprise polysilicon and have a width ranging from about 100 Å to about 500 Å.

18. (original) The non-volatile memory device of claim 14, further comprising:

a dielectric cap formed on the top surface of the conductive fin.

19. (original) The non-volatile memory device of claim 14, wherein the oxide layer acts as a tunnel oxide for the memory device and the width of the oxide layer ranges from about 10 Å to about 100 Å.

20. (original) The non-volatile memory device of claim 14, wherein the insulating layer comprises a buried oxide layer and the conductive fin comprises at least one of silicon and germanium.

21. (currently amended) A memory device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin structure formed on the insulating layer, the fin structure having a first and second side surface;

an oxide layer having a width ranging from about 10 Å to about 100 Å formed on the first and second side surfaces of the fin structure, the oxide layer acting as a tunnel oxide layer for the memory device;

a first spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the first side surface of the fin structure, the first spacer acting as a first floating gate for the memory device;

a second spacer having a width ranging from about 100 Å to about 500 Å formed adjacent the second side surface of the fin structure, the second spacer acting as a second floating gate for the memory device;

a gate dielectric layer formed on the first and second spacers;

a first gate ~~formed on~~ contacting the insulating layer and disposed on a first side of the fin;

a second gate ~~formed on~~ contacting the insulating layer and disposed on a second side of the fin opposite the first side, wherein the first and second gates are electrically isolated from each other;

a source region formed on the insulating layer adjacent a first end of the fin structure; and

a drain region formed on the insulating layer adjacent a second end of the fin structure opposite the first end.

22. (previously presented) The memory device of claim 21, wherein the gate dielectric comprises an oxide having a thickness ranging from about 50 Å to about 200 Å.